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(54) **Semiconductor laser having electro-static discharge protection**

Halbleiterlaser mit Schutz gegen elektrostatische Entladungen

Laser à semi-conducteur protégé contre des décharges électrostatiques

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- **PATENT ABSTRACTS OF JAPAN vol. 006, no. 103 (E-112), 12 June 1982 (1982-06-12) & JP 57 034380 A (NEC CORP), 24 February 1982 (1982-02-24)**
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Description

Field of the Invention

[0001] The present invention pertains, in general, to lasers and, more particularly, to vertical cavity surface emitting lasers.

Background of the Invention

[0002] Recently, there has been an increased interest in a new type of laser device called a vertical cavity surface emitting laser (VCSEL). Several advantages of VCSEL devices are apparent, such as having a circular beam, two-dimensional array capability, and allowing wafer scale testing. These advantages are due in part from advances in metal organic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE) that allow monolithic growth of diffractive Bragg reflectors (DBRs) for VCSELs.

[0003] However, even with these advantages, VCSEL devices are more susceptible to electro-static discharge (ESD) events because of smaller active volume. Electro-static discharge events are events where a high static charge is built up and subsequently discharged. When the high static charge discharges through a VCSEL, it will be catastrophically damaged. Thus, conventional VCSEL's are limited to applications that are not susceptible to ESD events, which reduces the number of possible applications for VCSEL's.

[0004] JP 9 027 657 A discloses a PN junction diode of reverse direction formed in parallel with a semiconductor laser on the same substrate.

[0005] Thus it is highly desirable and an object of the present invention to provide a protective circuitry to increase the VCSEL ESD damage threshold.

[0006] It is another purpose of the present invention to provide for a method to integrate the protective diode with the VCSELs.

Summary of the Invention

[0007] The above problems and others are at least partially solved and the above objects are realized in a semiconductor laser having electro-static discharge (ESD) protection. To provide the ESD protection, a vertical cavity surface emitting laser (VCSEL) is fabricated and a diode is fabricated and connected in parallel reverse orientation to the VCSEL. When a reverse biased ESD event is applied to the VCSEL, the parallel connected diode will provide a very low resistance path to quickly drain off the charge before it can damage the VCSEL. Since the reverse biased ESD damage threshold is typically lower than the forward biased ESD damage threshold, the proposed solution will increase the VCSEL ESD tolerence level to the forward biased ESD damage threshold level. The parallel connected diode is fabricated adjacent and in the same fabrication steps in which the VCSEL is formed. Thus, very little extra chip real estate is required and no extra fabrication steps are required to provide the protection.

[0008] A VCSEL and a method of fabricating the VCSEL are defined in claims 1 and 2.

Brief Description of the Drawings

[0009]

FIG. 1 is an enlarged isometric diagram of a semiconductor substrate having a VCSEL and a diode coupled thereto, wherein the VCSEL and the diode are also shown in section;
FIG. 2 is a view in top plan of the structure of FIG. 1;
FIG. 3 is an equivalent circuit of a VCSEL coupled to a diode.

Detailed Description of the Drawings

[0010] FIG. 1 is an enlarged isometric diagram of a semiconductor substrate 101 with a surface 107 having a VCSEL 103 and a diode 105 coupled thereto, wherein VCSEL 103 and diode 105 are also shown in section. VCSEL 103 and diode 105 are made including several features or elements, such as substrate 101, a stack 109 of distributed Bragg reflectors (DBRs), an active area 111 having a cladding region 113, an active region 115, a cladding region 117, a stack 119 of distributed Bragg reflectors (DBRs) having a surface 120, a dielectric layer 121, and conductive layers 123 and 125.

[0011] It should be understood that FIG. 1 is a sectional view of VCSEL 103 and diode 105, with portions thereof broken away and shown in section to illustrate the inner construction. Also, FIG. 2 is a view in top plan illustrating the overall relationship between the various components. VCSEL 103 and diode 105 can represent one of a plurality of VCSELs that make up an array. Additionally, it should be understood that FIG. 1 has been simplified, thus purposely omitting some engineering details so as to more clearly illustrate the present invention.

[0012] For purposes of orienting the reader, a brief description of materials and methods is provided hereinbelow. VCSEL 103 and diode 105 are fabricated on any suitable substrate, such as gallium arsenide, silicon, indium gallium phosphide, or the like having surface 107. Generally, surface 107 of substrate 101 is processed to form several epitaxial layers including stack 109, active area 111 including cladding region 113, active region 115, and cladding region 117, and stack 119. Stack 109, active area 111, and stack 119 are made by any suitable epitaxial method, such as MBE, MOVPE, or the like.

[0013] Once stack 109, active area 111, and stack 119 have been formed, trenches 131, 133, 135, and 137 are formed by any suitable process or combination of processes, such as photolithography, etching, or the like. Trench 131 defines VCSEL 103 and isolates a portion

of stack 119 to confine a current path through stack 109, active area 111, and stack 119. Trench 131 extends from surface 120 of stack 119 to just above active area 111. Thus, when current flows, active region 115 is activated, thereby generating light which is reflected by stacks 109 and 119 for lasing and ultimately emitted through an orifice 122.

[0014] Trench 133 defines diode 105 and isolates diode 105 from VCSEL 103 and the rest of substrate 101. Trench 133 extends from surface 120 through the various layers and into substrate 101. Diode 105 is further processed to expose a portion 145 of stack 109 by any suitable method or combination of methods such as photolithography, etching or the like, thereby exposing portion 145 to be used as an electrical contact.

[0015] It should be understood by one of ordinary skill in the art that the fabrication of trenches 131, 133, 135, and 137 is not generally accomplished as a single step but rather is achieved by using a plurality of steps. Additionally, it will be understood by one of ordinary skill in the art that sizing, i.e., widths and depths of trenches 131, 133, 135, and 137 is application specific and can range widely in accordance with specific design requirements, including but not limited to materials utilized, operating voltages and frequencies, etc..

[0016] However, by way of example only, with regard to trench 131, trench 131 has a width 150 ranging from 0.1 micron to 100 microns and a depth 151 ranging from 0.1 micron to just above cladding region 117. Trench 133 has a width 153 ranging from 0.1 micron to about 100 microns and a depth extending from surface 120 into substrate 101. Trench 135 has a width sufficient to expose a useable contact surface of stack 109 and a depth extending from surface 120 into stack 109. Trench 137 has a width 155 ranging from 0.1 micron to about 100 microns and a depth extending from surface 120 to just below active area 111 or into substrate 101.

[0017] Once trenches 131, 133, 135, and 137 have been formed, dielectric layer 121 is disposed on the exposed surfaces of the structure. Dielectric layer 121 includes any suitable dielectric material, such as nitride, oxynitride, oxide, or the like. It will be understood by one of ordinary skill in the art that disposition of dielectric layer 121 can be achieved using either an additive method, i.e., using a combination of techniques such as photolithography and deposition or a subtractive method, i. e., using a combination of techniques such as depositions, photolithography and etching, thereby patterning and positioning portions of dielectric layer 121 in their correct positions.

[0018] For example, with dielectric layer 121 being made of nitride and deposited over surface 120 after the fabrication of trenches 131, 133, 135, and 137, dielectric layer 121 is patterned with a masking material. The masking material exposes certain areas or portions of the dielectric layer. In this specific case, areas 145, 157, 159, 161, 163, and 171 of dielectric layer 121 are exposed. Once areas 145, 157, 159, 161, 163, and 171 are exposed, an etch process is done to remove exposed areas 145, 157, 159, 161, 163, and 171 of dielectric layer 121, thereby exposing portions of stacks 109 and 119.

[0019] Any suitable etch process or combination of etch processes can be used to remove areas 145, 157, 159, 161, 163 and 171 of dielectric layer 121. For example, if dielectric layer 121 is made of nitride, a dry etch, i.e., a fluorine based plasma chemistry can be used. Additionally, a wet etch, i.e., a HF solution could also be used. It will be understood by one of ordinary skill in the art that etch chemistries and techniques vary depending upon the materials involved.

[0020] Once areas 145, 157, 159, 161, 163 and 171 of stacks 109 and 119 are exposed, conductive layers 123 and 125 are disposed on substrate 101. Conductive layers 123 and 125 are formed of any suitable material, such as a metal, e.g., aluminum, gold, silver, or the like, or an alloy, e.g., aluminum/copper, gold/zinc, gold/germanium, titanium/tungsten, or the like, or doped material, e.g., doped poly-silicon. Further, conductive layers 123 and 125 can be disposed on substrate 101 by any suitable method, such as sputtering, evaporation, chemical vapor deposition, or the like.

[0021] Once conductive layers 123 and 125 are disposed on substrate 101, conductive layers 123 and 125 are patterned by any suitable method as previously described with reference to dielectric layer 121. A pattern is made of a masking material which covers portions of conductive layers 123 and 125 and exposes other portions of conductive layers 123 and 125. Once conductive layers 123 and 125 are patterned with the masking material, the exposed portions of conductive layer 123 and 125 are etched, thereby removing the exposed portions of conductive layers 123 and 125, and exposing portions of dielectric layer 121.

[0022] As shown in FIG. 1, conductive portion 164 includes a conductive bonding pad 166, a conductive lead 167 and an upper terminal for VCSEL 103. Generally, conductive bonding pad 166 acts as an electrical connection for applying an external voltage to the upper terminal of VCSEL 103 and an opposite terminal of diode 105. From conductive bonding pad 166, conductive lead 167 electrically couples stack 119 of VCSEL 103 with contact 145 of stack 109.

[0023] Conductive portion 169 provides an external connection pad for electrical connections to the upper terminal of diode 105 (portion 171) and electrically connects the lower terminal of VCSEL 103 (portions 161 and 163 and stack 109) to the upper terminal of diode 105. By electrically coupling the conductive portion 164 to VCSEL 103 and portion 145, and electrically coupling conductive portion 169 to portions 159, 161, 163, and 171, diode 105 is electrically coupled in reverse parallel to VCSEL 103. By placing diode 105 in reverse parallel with VCSEL 103, a reverse biased ESD protection is achieved. In an ESD event, with the reverse biased diode 105 connected in parallel to VCSEL 103, the charge

is drained off into substrate 101 through diode 105.

[0024] FIG. 3 is a schematic diagram of VCSEL 103 coupled to diode 105. VCSEL 103 includes electrical terminals 203 and 205 and diode 105 includes electrical terminals 207 and 209. It will be understood that diode 105 can be fabricated in a variety of embodiments but in the preferred embodiment diode 105 is a p-i-n diode. Further, depending upon materials, etc. the breakdown voltage of diode 105 can be a relatively wide range but should be at least sufficient to withstand and discharge any expected ESD events. Generally the range of breakdown voltages can be from 10s to several hundred volts. VCSEL 103 and diode 105 are electrically coupled at contacts 210 and 211. By electrically coupling VCSEL 103 with diode 105, the reverse biased ESD damage threshold of VCSEL 103 is increased to at least the level of the forward biased ESD damage threshold, which is typically at least 100 - 200 Volts higher. Thus, the reliability of VCSEL 103 is improved due to the decreasing likelihood of catastrophic failure of VCSEL 103 by an ESD event.

[0025] By now it should be appreciated that a novel article and method of making has been provided. A vertical cavity surface emitting laser having higher reliability, with improved performance has been described. These and other advantages result from the electrical coupling of a diode with a vertical cavity surface emitting diode. Further, the VCSEL and protective diode are formed during the same process so that no additional steps or labor is required and the diode uses very little extra chip real estate so that it is very inexpensive to integrate with the VCSEL.

[0026] While we have shown and described specific embodiments of the present invention, further modifications and improvement will occur to those skilled in the art. We desire it to be understood, therefore, that this invention is not limited to the particular forms shown and we intend in the appended claims to cover all modifications that do not depart from the scope of this invention.

Claims

1. A vertical cavity surface emitting laser comprising:

   a substrate (101);
   a first distributed Bragg reflector (109) disposed on the substrate, the first distributed Bragg reflector including a plurality of alternating layers;
   an active area (111) overlying the first distributed Bragg reflector;
   a second distributed Bragg reflector (119) having a surface overlying the active area, the second distributed Bragg reflector including a plurality of alternating layers;
   a first trench (131) having a first width and a first depth, wherein the first depth of the first trench extends into a portion of the second distributed Bragg reflectors and defines a vertical cavity surface emitting laser;
   a second trench (133) with a second width and a second depth, wherein the second depth of the second trench extends into a portion of the substrate, the second trench defines and isolates a diode (105) having a diode structure; and
   a third trench (135) having a third width and a third depth less than the second depth, wherein the third trench is located inside the second trench and extends into contact with the first distributed Bragg reflector such that a horizontal portion (145) of the first distributed Bragg reflector adjacent the active layer in the diode structure is exposed;
   a fourth trench (137) having a fourth width and a fourth depth, wherein the fourth depth extends into contact with the first distributed Bragg reflector of the diode structure such that a portion (163) of the first distributed Bragg reflector (109) is exposed;
   a dielectric layer (121) covering the surface of the second stack of distributed Bragg reflectors, the dielectric layer defining an opening (157) adjacent the first trench region (131) exposing a portion of the second distributed Bragg reflector (119), exposing the horizontal portion (145) of the diode's first distributed Bragg reflector (109) in the third trench (135) adjacent the active area (111) and defining an opening (171) exposing a contact through the second distributed Bragg reflector (119) of the diode; and
   a first metal layer (123) electrically connecting the exposed portion (157) of the second distributed Bragg reflector adjacent the first trench (131) with the horizontal portion (145) of the first distributed Bragg reflector adjacent the active area in the third trench (135) and a second metal layer (169) electrically connecting the exposed portion (163) of the first distributed Bragg reflector in the fourth trench (137) with the exposed portion of the second distributed Bragg reflector of the diode.

2. A method of fabricating a vertical cavity semiconductor laser with electrostatic discharge protection as claimed in claim 1, the method comprising:

   providing a substrate (101);
   depositing a first distributed Bragg reflector (109) on the substrate, an active region (115) on the first distributed Bragg reflector, and a second distributed Bragg reflector (119) on the active region;
   etching trenches (131, 133) in the first distrib-

uted Bragg reflector, the active region, and second distributed Bragg reflector defining a vertical cavity surface emitting laser (103) and a diode (105) isolated from the vertical cavity surface emitting laser;
covering exposed surfaces of the trenches and the second distributed Bragg reflector with a dielectric layer (121);
defining openings in the dielectric layer in communication with opposite terminals of the vertical cavity surface emitting laser and the diode; and
depositing a metal layer (123) on the dielectric layer and in the openings to connect the diode in reverse parallel with the vertical cavity surface emitting laser.

Patentansprüche

1. Oberflächenemittierender Laser mit vertikalem Resonator, der aufweist:

ein Substrat (101);
einen auf dem Substrat angeordneten ersten verteilten Bragg-Reflektor (109), wobei der erste verteilte Bragg-Reflektor eine Mehrzahl wechselnder Schichten umfasst;
einen aktiven Bereich (111), der über dem ersten verteilten Bragg-Reflektor liegt;
einen zweiten verteilten Bragg-Reflektor (119) mit einer Oberfläche, die über dem aktiven Bereich liegt, wobei der zweite verteilte Bragg-Reflektor eine Mehrzahl wechselnder Schichten umfasst;
einen ersten Graben (131) mit einer ersten Breite und einer ersten Tiefe, wobei sich die erste Tiefe des ersten Grabens in einen Abschnitt des zweiten verteilten Bragg-Reflektors erstreckt und einen oberflächenemittierenden Laser mit vertikalem Resonator definiert;
einen zweiten Graben (133) mit einer zweiten Breite und einer zweiten Tiefe, wobei sich die zweite Tiefe des zweiten Grabens in einen Abschnitt des Substrates erstreckt, und wobei der zweite Graben eine Diode (105) definiert und isoliert, die eine Diodenstruktur aufweist; und
einen dritten Graben (135) mit einer dritten Breite und einer dritten Tiefe, die kleiner als die zweite Tiefe ist, wobei der dritte Graben innerhalb des zweiten Grabens angeordnet ist und sich bis zum Kontakt mit dem ersten verteilten Bragg-Reflektors derart erstreckt, dass ein waagerechter Abschnitt (145) des ersten verteilten Bragg-Reflektors benachbart zu dem aktiven Bereich in der Diodenstruktur freigelegt wird;
einen vierten Graben (137) mit einer vierten Breite und einer vierten Tiefe, wobei sich die vierte Tiefe bis zum Kontakt mit dem ersten verteilten Bragg-Reflektor der Diodenstruktur derart erstreckt, dass ein Abschnitt (163) des ersten verteilten Bragg-Reflektors (109) freigelegt wird;
eine dielektrische Schicht (121), welche die Oberfläche des zweiten Stapels der verteilten Bragg-Reflektoren abdeckt, wobei die dielektrische Schicht eine zu dem Bereich des ersten Grabens (131) benachbarte Öffnung (122) definiert, einen Abschnitt des zweiten verteilten Bragg-Reflektors (119) freilegt, den waagerechten Abschnitt (145) des ersten verteilten Bragg-Reflektors (109) der Diode in dem dritten Graben (135) benachbart zu dem aktiven Bereich (111) freilegt, und eine Öffnung (171) definiert, die einen Kontakt durch den zweiten verteilten Bragg-Reflektor (119) der Diode freilegt; und
eine erste Metallschicht (123), die den freigelegten zu dem ersten Graben (131) benachbarten Abschnitt (157) des zweiten verteilten Bragg-Reflektors mit dem waagerechten Abschnitt (145) des ersten verteilten Bragg-Reflektors in dem dritten Graben elektrisch verbindet, und eine zweite Metallschicht (169), die die den freigelegten Abschnitt (163) des ersten Bragg-Reflektors in dem vierten Graben (137) mit dem freigelegten Teil des zweiten verteilten Bragg-Reflektors der Diode elektrisch verbindet.

2. Verfahren zur Herstellung eines Halbleiterlasers mit vertikalem Resonator mit Schutz vor elektrostatischer Entladung nach Anspruch 1, wobei das Verfahren umfasst:

Bereitstellen eines Substrates (101);
Aufbringen eines ersten verteilten Bragg-Reflektors (109) auf das Substrat, eines aktiven Bereichs (115) auf den ersten verteilten Bragg-Reflektor und eines zweiten verteilten Bragg-Reflektors (119) auf den aktiven Bereich;
Ätzen von Gräben (131, 133) in den ersten verteilten Bragg-Reflektor, den aktiven Bereich, und den zweiten verteilten Bragg-Reflektor, um einen oberflächenemittierenden Laser (103) mit vertikalem Resonator und eine Diode (105) zu definieren, die von dem oberflächenemittierenden Laser mit vertikalem Resonator isoliert ist;
Abdecken von freigelegten Oberflächen der Gräben und des zweiten verteilten Bragg-Reflektors mit einer dielektrischen Schicht (121);
Definieren von Öffnungen in der dielektrischen Schicht, die in Verbindung mit gegenüberliegenden Anschlüssen des oberflächenemittie-

renden Lasers mit vertikalem Resonator und der Diode stehen; und
Aufbringen einer Metallschicht (123) auf die dielektrische Schicht und in den Öffnungen, um die Diode entgegengesetzt parallel mit der oberflächenemittierenden Laserdiode mit vertikalem Resonator zu verbinden.

Revendications

1. Laser à cavité verticale et à émission par la surface, comprenant :

un substrat (101) ;

un premier réflecteur de Bragg distribué (109) disposé sur le substrat, le premier réflecteur de Bragg distribué comprenant une pluralité de couches disposées en alternance ;

une région active (111) recouvrant le premier réflecteur de Bragg distribué ;

un deuxième réflecteur de Bragg distribué (119) ayant une surface recouvrant la région active, le deuxième réflecteur de Bragg distribué comprenant une pluralité de couches disposées en alternance ;

une première tranchée (131) ayant une première largeur et une première profondeur, la première profondeur de la première tranchée s'étendant dans une partie du deuxième réflecteur de Bragg distribué et définissant un laser à cavité verticale et à émission par la surface ;

une deuxième tranchée (133) ayant une deuxième largeur et une deuxième profondeur, la deuxième profondeur de la deuxième tranchée s'étendant dans une partie du substrat, et la deuxième tranchée définissant et isolant une diode (105) ayant une structure de diode ; et

une troisième tranchée (135) ayant une troisième largeur et une troisième profondeur inférieure à la deuxième profondeur, la troisième tranchée étant située à l'intérieur de la deuxième tranchée et s'étendant en contact avec le premier réflecteur de Bragg distribué, de telle sorte qu'une partie horizontale (145) du premier réflecteur de Bragg distribué, contiguë à la couche active dans la structure de diode, soit exposée ;

une quatrième tranchée (137) ayant une quatrième largeur et une quatrième profondeur, la quatrième profondeur s'étendant en contact avec le premier réflecteur de Bragg distribué de la structure de diode, de telle sorte qu'une partie (163) du premier réflecteur de Bragg distribué (109) soit exposée ;

une couche diélectrique (121) recouvrant la surface de la deuxième pile de réflecteurs de Bragg distribués, la couche diélectrique définissant une ouverture (122) contiguë à la première région de tranchée (131), qui expose une partie du deuxième réflecteur de Bragg distribué (119), exposant la partie horizontale (145) du premier réflecteur de Bragg distribué (109) de la diode, dans la troisième tranchée (135), qui est contiguë à la région active (111), et définissant une ouverture (171) exposant un contact à travers le deuxième réflecteur de Bragg distribué (119) de la diode ; et

une première couche métallique (123) connectant électriquement la partie exposée (157) du deuxième réflecteur de Bragg distribué qui est contiguë à la première tranchée (131) avec la partie horizontale du premier réflecteur de Bragg distribué qui est contiguë à la région active dans la troisième tranchée (135), et une deuxième couche métallique (169) connectant électriquement la partie exposée du premier réflecteur de Bragg distribué dans la quatrième tranchée (137) avec la partie exposée du deuxième réflecteur de Bragg distribué de la diode.

2. Procédé de fabrication d'un laser à cavité verticale et à émission par la surface ayant une protection contre les décharges électrostatiques selon la revendication 1, le procédé comprenant les étapes qui consistent à :

se procurer un substrat (101) ;

déposer un premier réflecteur de Bragg distribué (109) sur le substrat, une région active (115) sur le premier réflecteur de Bragg distribué, et un deuxième réflecteur de Bragg distribué (119) sur la région active ;

graver des tranchées (131, 133) dans le premier réflecteur de Bragg distribué, la région active et le deuxième réflecteur de Bragg distribué, définissant un laser à cavité verticale et à émission par la surface (103) et une diode (106) isolée du laser à cavité verticale et à émission par la surface ;

recouvrir des surfaces exposées des tranchées et du deuxième réflecteur de Bragg distribué avec une couche diélectrique (121) ;

définir des ouvertures dans la couche diélectrique en communication avec des bornes opposées du laser à cavité verticale et à émission par la surface et de la diode ; et

déposer une couche métallique (123) sur la couche diélectrique et dans les ouvertures, pour connecter la diode en parallèle inverse avec le laser à cavité verticale et à émission par la surface.

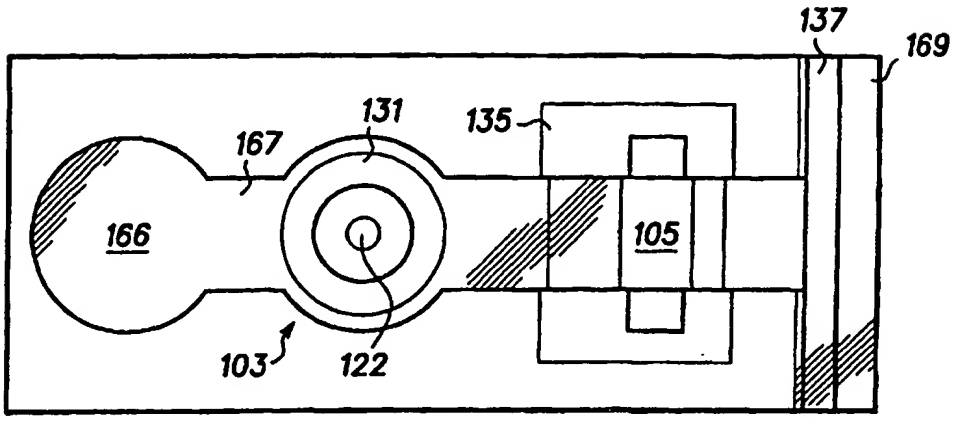

FIG. 1

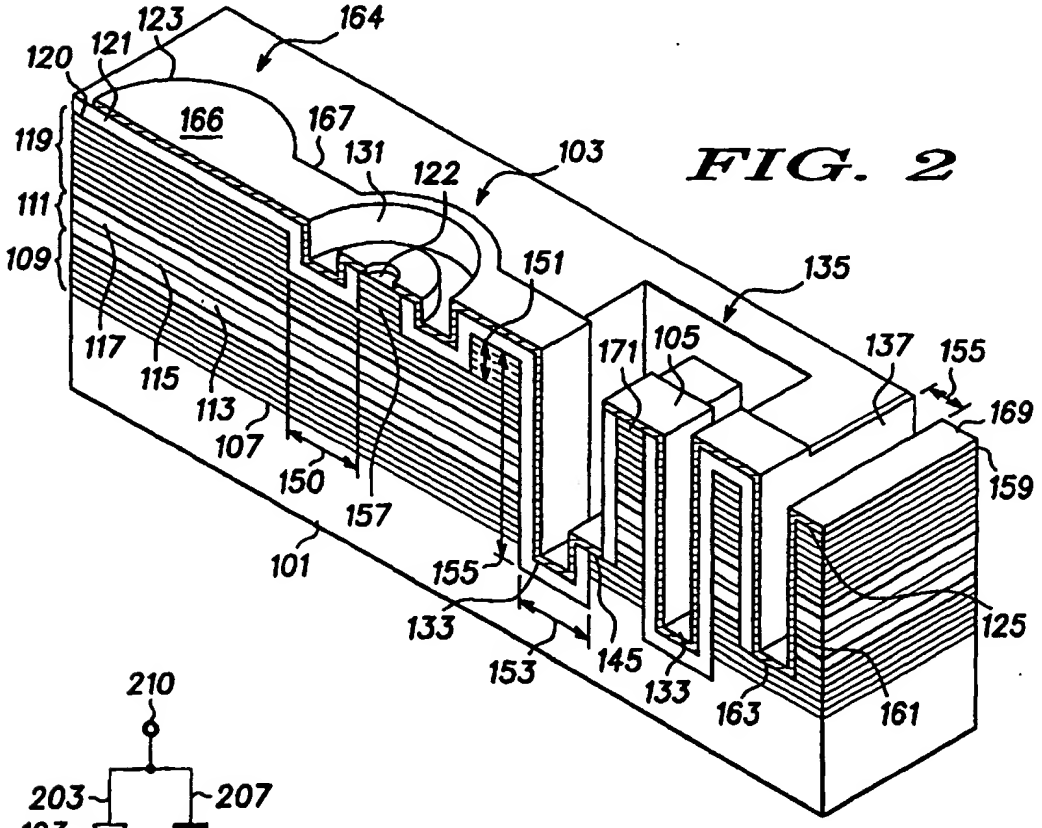

FIG. 2

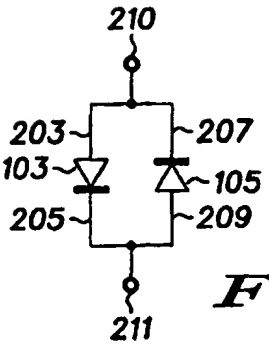

FIG. 3